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EXAMINER	
TAYONG, HELENE E	

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2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/725,974	SAVEKAR ET AL.	
	Examiner	**Art Unit**	
	HELENE TAYONG	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _06/18/09_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-18 and 22-24_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-18 and 22-24_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _02 December 2003_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on 06/18/09. Claims 1-18 and 22-24 are pending in this application and have been considered below.

Response to Arguments

2. Applicant's arguments with respect to rejection of claims 1-6, 11-12 and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kono et al (US 20010005398 A1) in view of Tada (US 7142776) have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with respect to claims I, 6 and I3 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims I ,3 , 4 and 5 copending Application No. 10914808 has been reviewed and Applicant has submitted a terminal disclaimer, rejection withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6, 11-18 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kono et al (US 20010005398 A1) in view of Wu et al (US 6473558).

(1) with regards to claims 1 and 13;

Kono et al teaches a method (Fig .6) for displaying images on a display comprising:

a decoder (52) for decoding encoded images and parameters associated with the images (pg.5, [0066], lines 3-5).

image buffers (58) for storing the decoded images (pg. 5, [0066], lines 7-10) ;

parameter buffers (53) for storing the decoded parameters associated with the decoded images(pg. 5, [0067], lines 2-6) ; and

Kono discloses a display manager (55) and decode control section (64), but does not explicitly teach **determining when to overwrite an existing image in the image buffers and providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer wherein the decoder overwrites the existing image after receiving the signal**.

Kono discloses a frame memory in (fig. 6, 53) with three banks, bank 1, bank 2 and bank 3. Data is transferred (read/written fig. 7, steps S3-S7) from the display control section (55) and MB buffer (58) in to the frame buffer, Kono is not explicit about **determining when to overwrite an existing image in the image buffers and providing a signal to the decoder indicating when to overwrite**

the existing image in the frame buffer wherein the decoder overwrites the existing image after receiving the signal.

However, Wu et al in the same endeavor (figs.1, 2) discloses a system for displaying a series of video frames in reverse order. Fig. 4 shows three frame buffers M1, M2 and M3 into the desired order of display. Frame pointers (F, for forward, B for backward, and C for current) are used to direct the decoded frame into a memory location (col. 8, lines 44-46). On col. 10, lines 9-24, line 530 shows the desired assignment of the anchor frames into the three frame buffers M1,M2 and M3. AS shown in line 530, frames Io and p3 are decoded first. They are not, however, yet displayed but stored in frame buffers M1 and M2. The chronologically last frame in the nine frame from sequence, p6 is decoded in the third cycle. It is displayed immediately thereafter, as shown in line 540. On subsequent cycles, frame p3 and frame Io are displayed and as shown in line 530, and their **frame buffers are immediately overwriiten with newly decoded frames** (fig. 5).

As discussed in the back ground section of Wu et al, the memory is a major cost item in the production of video encoders, and generally memories with higher band widths cost more. Thus, it is desirable to reduce the memory bandwidth requirements of the encoder system as much as possible to either reduce or allow for increased performance (col. 5, lines 16-21). It would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized the method as taught by Wu et al in a manner as claimed in this invention for the benefit of smoothly displaying MPEG video while minimizing the required

quantity of memory for temporary storage (col. 5, lines 41-44).

(2) with regards to claim 2;

Kono further discloses wherein the set of parameters (pg. 5, [0067], lines 2-6) includes a parameter indicating when the system is utilizing a technique requiring selective images to be displayed more than once (pg. 6, [0086], lines 7-11).

(3) with regards to claim 3 ;

Kono further discloses wherein the system for displaying images on a display (fig.6) further comprises:

a first processor (54);

a second processor (55);

a first memory (58);

a second memory(53); and

wherein the first memory stores an instruction set for the decoder (pg.6, [0079]).

(4) with regards to claim 4;

Kono further discloses wherein the first processor (54) executes the instruction for the decoder (pg. 6, [0081] lines 3-4).

(5) with regards to claim 5;

Kono further discloses wherein the second memory stores (53) an instruction set for the display manager (pg.6, [0085], lines 6-8), the instruction set

for the display manager (fig.6, 68) executed by the second processor (pg.6, [0085], lines 8-11).

(6) with regards to claim 6;

Kono further discloses wherein the second processor (55) determines when to overwrite the existing image (pg. 6, [0084]-[0086]).

(7) with regards to claim 11;

Kono further discloses the second memory stores the image buffers (fig. 6, 53d), (pg. 5, [0067]).

(8) with regards to claim 12;

Kono further discloses wherein the second memory stores the parameter buffers (fig. 6, 53e), (pg. 6 [0067).

(9) with regards to claim 14;

Kono further discloses wherein execution of the instructions by the first processor further causes: displaying the images (fig. 7 and fig.8).

(10) with regards to claim 15;

Kono further discloses a second processor connected to the integrated circuit (fig, 6, 55); and

a second memory connected to the processor (fig. 6, 53), the second

memory storing instructions, wherein execution of the instructions by the second processor causes:

Kono discloses a display manager (55) and decode control section (64), but does not explicitly teach **determining when to overwrite an existing image in the image buffers and providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer wherein the decoder overwrites the existing image after receiving the signal**.

Kono discloses a frame memory in (fig. 6, 53) with three banks, bank 1, bank 2 and bank 3. Data is transferred (read/written fig. 7, steps S3-S7) from the display control section (55) and MB buffer (58) in to the frame buffer, Kono is not explicit about **determining when to overwrite an existing image in the image buffers and providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer wherein the decoder overwrites the existing image after receiving the signal.**

However, Wu et al in the same endeavor (figs.1, 2) discloses a system for displaying a series of video frames in reverse order. Fig. 4 shows three frame buffers M1, M2 and M3 into the desired order of display. Frame pointers (F, for forward, B for backward, and C for current) are used to direct the decoded frame into a memory location (col. 8, lines 44-46). On col. 10, lines 9-24, line 530 shows the desired assignment of the anchor frames into the three frame buffers M1,M2 and M3. AS shown in line 530, frames Io and p3 are decoded first. They are not, however, yet displayed but stored in frame buffers M1 and M2. The chronologically last frame in the nine frame from sequence, p6 is decoded in the

third cycle. It is displayed immediately thereafter, as shown in line 540. On subsequent cycles, frame p3 and frame Io are displayed and as shown in line 530, and their **frame buffers are immediately overwriiten with newly decoded frames** (fig. 5).

As discussed in the back ground section of Wu et al, the memory is a major cost item in the production of video encoders, and generally memories with higher band widths cost more. Thus, it is desirable to reduce the memory bandwidth requirements of the encoder system as much as possible to either reduce or allow for increased performance (col. 5, lines 16-21). It would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized the method as taught by Wu et al in a manner as claimed in this invention for the benefit of smoothly displaying MPEG video while minimizing the required quantity of memory for temporary storage (col. 5, lines 41-44).

(11) with regards to claim 16;

Kono further discloses wherein execution of the instructions in the first memory by the first processor further causes: decoding parameters associated with the images (pg.6, [0080]).

(12) with regards to claim 17;

Kono further discloses examining some of the decoded parameters associated with the images by the second processor (pg. 6, [0085], lines 10-11).

(13) with regards to claim 18;

Kono further discloses a parameter buffer (53) connected to the integrated circuit and a frame buffer connected to the integrated circuit (fig.6), wherein the parameter buffer stores the decoded parameters(pg. 5, [0067], lines 2-6), and the frame buffer stores the decoded images (pg. 5, [0067], lines 2-6).

(14) with regards to claim 22;

Kono discloses wherein the (display manager and decoding section) in fig. 6, 55 and 64) but does not explicitly teach determines when to overwrite an existing image in the image buffer based at least in part on at least one of the decoded parameters.

Kono discloses a frame memory in (fig. 6, 53) with three banks, bank 1, bank 2 and bank 3. Data is transferred (read/written fig. 7, steps S3-S7) from the display control section (55) and MB buffer (58) in to the frame buffer, Kono is not explicit about **determining when to overwrite an existing image in the image buffers and providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer wherein the decoder overwrites the existing image after receiving the signal.**

However, Wu et al in the same endeavor (figs.1, 2) discloses a system for displaying a series of video frames in reverse order. Fig. 4 shows three frame buffers M1, M2 and M3 into the desired order of display. Frame pointers (F, for forward, B for backward, and C for current) are used to direct the decoded frame into a memory location (col. 8, lines 44-46). On col. 10, lines 9-24, line 530

shows the desired assignment of the anchor frames into the three frame buffers M1,M2 and M3. AS shown in line 530, frames Io and p3 are decoded first. They are not, however, yet displayed but stored in frame buffers M1 and M2. The chronologically last frame in the nine frame from sequence, p6 is decoded in the third cycle. It is displayed immediately thereafter, as shown in line 540. On subsequent cycles, frame p3 and frame Io are displayed and as shown in line 530, and their **frame buffers are immediately overwriiten with newly decoded frames** (fig. 5).

As discussed in the back ground section of Wu et al, the memory is a major cost item in the production of video encoders, and generally memories with higher band widths cost more. Thus, it is desirable to reduce the memory bandwidth requirements of the encoder system as much as possible to either reduce or allow for increased performance (col. 5, lines 16-21). It would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized the method as taught by Wu et al in a manner as claimed in this invention for the benefit of smoothly displaying MPEG video while minimizing the required quantity of memory for temporary storage (col. 5, lines 41-44).

(15) with regards to claim 23;

Kono discloses wherein the (display manager and decoding section) in fig. 6, 55 and 64) but does not explicitly teach determines when to overwrite an existing image based on the parameter indicating when the system is utilizing the technique requiring selective images to be displayed more than once.

Kono discloses a frame memory in (fig. 6, 53) with three banks, bank 1, bank 2 and bank 3. Data is transferred (read/written fig. 7, steps S3-S7) from the display control section (55) and MB buffer (58) in to the frame buffer, Kono is not explicit about **determining when to overwrite an existing image in the image buffers and providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer wherein the decoder overwrites the existing image after receiving the signal.**

However, Wu et al in the same endeavor (figs.1, 2) discloses a system for displaying a series of video frames in reverse order. Fig. 4 shows three frame buffers M1, M2 and M3 into the desired order of display. Frame pointers (F, for forward, B for backward, and C for current) are used to direct the decoded frame into a memory location (col. 8, lines 44-46). On col. 10, lines 9-24, line 530 shows the desired assignment of the anchor frames into the three frame buffers M1,M2 and M3. AS shown in line 530, frames Io and p3 are decoded first. They are not, however, yet displayed but stored in frame buffers M1 and M2. The chronologically last frame in the nine frame from sequence, p6 is decoded in the third cycle. It is displayed immediately thereafter, as shown in line 540. On subsequent cycles, frame p3 and frame Io are displayed and as shown in line 530, and their **frame buffers are immediately overwriiten with newly decoded frames** (fig. 5).

As discussed in the back ground section of Wu et al, the memory is a major cost item in the production of video encoders, and generally memories with higher band widths cost more. Thus, it is desirable to reduce the memory

bandwidth requirements of the encoder system as much as possible to either reduce or allow for increased performance (col. 5, lines 16-21). It would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized the method as taught by Wu et al in a manner as claimed in this invention for the benefit of smoothly displaying MPEG video while minimizing the required quantity of memory for temporary storage (col. 5, lines 41-44).

(16) with regards to claim 24;

Kono discloses wherein the (display manager and decoding section) in fig. 6, 55 and 64) but does not explicitly teach determine when to overwrite an existing image with another image, wherein the another image and the existing image are from a same video sequence.

Kono discloses a frame memory in (fig. 6, 53) with three banks, bank 1, bank 2 and bank 3. Data is transferred (read/written fig. 7, steps S3-S7) from the display control section (55) and MB buffer (58) in to the frame buffer, Kono is not explicit about **determining when to overwrite an existing image in the image buffers and providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer wherein the decoder overwrites the existing image after receiving the signal.**

However, Wu et al in the same endeavor (figs.1, 2) discloses a system for displaying a series of video frames in reverse order. Fig. 4 shows three frame buffers M1, M2 and M3 into the desired order of display. Frame pointers (F, for forward, B for backward, and C for current) are used to direct the decoded frame

into a memory location (col. 8, lines 44-46). On col. 10, lines 9-24, line 530 shows the desired assignment of the anchor frames into the three frame buffers M1,M2 and M3. AS shown in line 530, frames Io and p3 are decoded first. They are not, however, yet displayed but stored in frame buffers M1 and M2. The chronologically last frame in the nine frame from sequence, p6 is decoded in the third cycle. It is displayed immediately thereafter, as shown in line 540. On subsequent cycles, frame p3 and frame Io are displayed and as shown in line 530, and their **frame buffers are immediately overwriiten with newly decoded frames** (fig. 5).

As discussed in the back ground section of Wu et al, the memory is a major cost item in the production of video encoders, and generally memories with higher band widths cost more. Thus, it is desirable to reduce the memory bandwidth requirements of the encoder system as much as possible to either reduce or allow for increased performance (col. 5, lines 16-21). It would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized the method as taught by Wu et al in a manner as claimed in this invention for the benefit of smoothly displaying MPEG video while minimizing the required quantity of memory for temporary storage (col. 5, lines 41-44).

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kono et al (US 20010005398 A1) in view of Wu et al (US 6473558) as applied in claim 6 above, and further in view of Vainsencher (US 5977997).

(1) with regards to claim 7;

Kono et al. discloses in (fig. 1) an integrated circuit comprises the first processor(115) and first memory (125a).

Kono et al modified by Wu et al fails to teach wherein the second processor is off-chip from the integrated circuit.

However, Vainsencher in the same field of endeavor (MPEG processing) teaches in (fig. 2) a computer system (200) wherein the second processor (202) is off-chip (single chip).

Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to have incorporated the this feature into the system of Kono, in the manner as claimed, for the benefit of increased opportunities for memory sharing (col.9, lines 13-14).

6. Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kono et al (US 20010005398 A1) in view of Wu et al (US 6473558) as applied in claim 3 above, and further in view of Vainsencher (US 5977997).

(1) with regards to claims 8;

Kono et al. discloses in (fig. 1) an integrated circuit comprises the first processor(115) and first memory (125a).

Kono et al as modified by Wu et al. fails to teach wherein the second processor is off-chip from the integrated circuit.

However, Vainsencher in the same field of endeavor (MPEG processing)

teaches in (fig. 2) a computer system (200) and where the second memory (fig. 2, 218) is an off-chip memory (single chip).

Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to have incorporated the this feature into the system of Kono, in the manner as claimed, for the benefit of increased opportunities for memory sharing (col.9, lines 13-14).

(2) with regards to claim 10;

Kono et al as modified by TWu et al. fails to teach where the second memory is DRAM.

However, Vainsencher in the same field of endeavor (MPEG processing) teaches in (fig. 2) a computer system (200) and where the second memory is DRAM (implicitly disclosed in the display controller) (col.9,13-24)).

Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to have incorporated the this feature into the system of Kono, in the manner as claimed, for the benefit of increased opportunities for memory sharing (col.9, lines 13-14).

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kono et al (US 20010005398 A1) in view of Wu et al (US 6473558) as applied in claim 3 above , and further in view of Xiang et al (US 20070153133 A1).

(1) with regards to claim 9;

Kono et al as modified by Wu et al discloses all of the subject matter

disclosed above but fails to teach wherein the first memory is a SRAM;

However, Xiang et al in the same field of endeavor teaches a SRAM (fig. 2, 204).

It would have been obvious to one of ordinary skill at the time of the invention to utilize the memory of Xiang et al in the method of Kono et al as modified by Wu et al. in order to provide a video processing system having a processing unit. The motivation to add Xiang et al 's memory in the method of Kono et al as modified by Wu et al. would be to generate random burst addresses for processing of video signal.

4. Claims 1, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kono et al (US 20010005398 A1) in view of Duruoz et al (US 6658056).

(1) with regards to claim 1 and 13;

Kono et al teaches a method (Fig .6) for displaying images on a display comprising:

a decoder (52) for decoding encoded images and parameters associated with the images (pg.5, [0066], lines 3-5).

image buffers (58) for storing the decoded images (pg. 5, [0066], lines 7-10) ;

parameter buffers (53) for storing the decoded parameters associated with the decoded images(pg. 5, [0067], lines 2-6) ; and

Kono discloses a display manager (55) and decode control section (64), but does not explicitly teach **determining when to overwrite an existing image in the image buffers and providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer wherein the decoder overwrites the existing image after receiving the signal**.

Kono discloses a frame memory in (fig. 6, 53) with three banks, bank 1, bank 2 and bank 3. Data is transferred (read/written fig. 7, steps S3-S7) from the display control section (55) and MB buffer (58) in to the frame buffer, Kono is not explicit about **determining when to overwrite an existing image in the image buffers and providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer wherein the decoder overwrites the existing image after receiving the signal.**

However, Duruoz et al in the same endeavor digital video decoding, buffering discloses in (fig. 3) DRAM buffer and Video decoder portions of the MPEG receiver. The picture decode control in fig. 3, 81 contains field sequence control software 80 which determines the order in which fields are to be decoded and when and to where in the buffer memory 78 decoded slices are to be written (col. 16, lines 27-45). In fig. 4D storage techniques which stores the rows of block in the next available rows of memory as the fields are successively sent to the display (col. 23, lines 10-32, col. 24, lines 21-55).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized the method as taught by Duruoz et al to overwrite when the memory is freed in a manner as claimed in this application for the

benefit of reducing cost of memory (col. 5, lines 23-27).

(2) with regards to claim 15;

Kono further discloses a second processor connected to the integrated circuit (fig, 6, 55); and

a second memory connected to the processor (fig. 6, 53), the second memory storing instructions, wherein execution of the instructions by the second processor causes:

Kono discloses a frame memory in (fig. 6, 53) with three banks, bank 1, bank 2 and bank 3. Data is transferred (read/written fig. 7, steps S3-S7) from the display control section (55) and MB buffer (58) in to the frame buffer, Kono is not explicit about **determining when to overwrite an existing image in the image buffers and providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer wherein the decoder overwrites the existing image after receiving the signal.**

However, Duruoz et al in the same endeavor digital video decoding, buffering discloses in (fig. 3) DRAM buffer and Video decoder portions of the MPEG receiver. The picture decode control in fig. 3, 81 contains field sequence control software 80 which determines the order in which fields are to be decoded and when and to where in the buffer memory 78 decoded slices are to be written (col. 16, lines 27-45). In fig. 4D storage techniques which stores the rows of block in the next available rows of memory as the fields are successively sent to the display (col. 23, lines 10-32, col. 24, lines 21-55).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have utilized the method as taught by Duruoz et al to overwrite when the memory is freed in a manner as claimed in this application for the benefit of reducing cost of memory (col. 5, lines 23-27).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, Schoner et al (US 5926227) discloses video decoding dynamic memory allocating system and method with error recovery.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HELENE TAYONG whose telephone number is (571)270-1675. The examiner can normally be reached on Monday-Friday 8:00 am to 5:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Liu Shuwang can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Helene Tayong/
Examiner, Art Unit 2611

August 25, 2009
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611